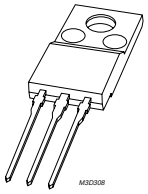


PHX3055E

TrenchMOS™ standard level FET

Rev. 03 — 18 March 2002 **Product data**

1. Description

N-channel standard level field-effect power transistor in a full pack using TrenchMOS™[1] technology.

Product availability:

PHX3055E in SOT186A (Isolated TO-220).

2. Features

- Fast switching
- Low on-state resistance
- Isolated mounting base.

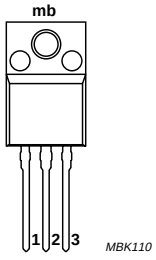
3. Applications

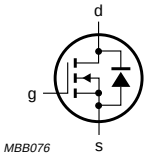
- DC to DC converters
- Switched mode power supplies.

4. Pinning information

Table 1: Pinning - SOT186A, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	drain (d)		
3	source (s)		
mb	mounting base		





SOT186A (Isolated TO-220)

1. TrenchMOS is a trademark of Koninklijke Philips Electronics.

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5. Quick reference data

Table 2: Quick reference data

Symbol	Parameter	Conditions		Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	25 °C ≤ T_j ≤ 150 °C		-	60	V
I_D	drain current (DC)	T_h = 25 °C; V_{GS} = 5 V	[1]	-	9	A
P_{tot}	total power dissipation	T_h = 25 °C	[1]	-	21	W
T_j	junction temperature			-	150	°C
R_{DSon}	drain-source on-state resistance	T_j = 25 °C; V_{GS} = 10 V; I_D = 5.5 A		120	150	mΩ

[1] Mounted to external heatsink, using heatsink compound.

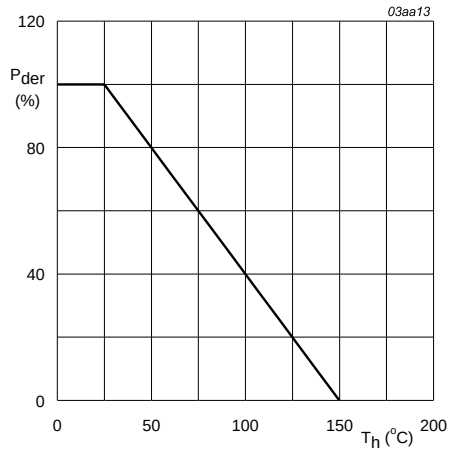
6. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

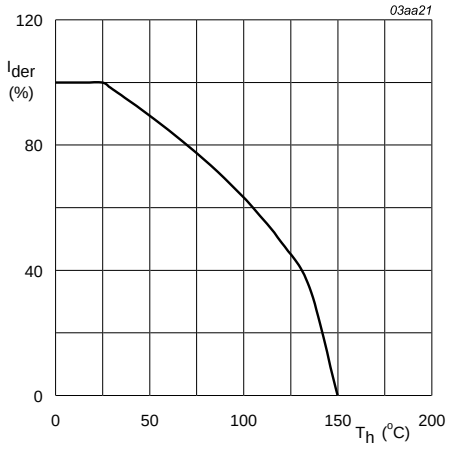
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage (DC)	25 °C ≤ T_j ≤ 150 °C		-	60	V
V_{DGR}	drain-gate voltage (DC)	25 °C ≤ T_j ≤ 150 °C; R_{GS} = 20 kΩ		-	60	V
V_{GS}	gate-source voltage (DC)			-	±20	V
I_D	drain current (DC)	T_h = 25 °C; V_{GS} = 10 V; Figure 2 and 3	[1]	-	9	A
		T_h = 100 °C; V_{GS} = 10 V; Figure 2	[1]	-	5.6	A
I_{DM}	peak drain current	T_h = 25 °C; pulsed; t_p ≤ 10 µs; Figure 3	[1]	-	36	A
P_{tot}	total power dissipation	T_h = 25 °C; Figure 1	[1]	-	21	W
T_{stg}	storage temperature			–55	+150	°C
T_j	operating junction temperature			–55	+150	°C
Source-drain diode						
I_S	source (diode forward) current (DC)	T_h = 25 °C	[1]	-	9	A
I_{SM}	peak source (diode forward) current	T_h = 25 °C; pulsed; t_p ≤ 10 µs	[1]	-	36	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive avalanche energy	unclamped inductive load; I_D = 3.3 A; t_{AL} = 0.22 ms; V_{DD} ≤ 25 V; R_{GS} = 50 Ω; V_{GS} = 10 V; starting T_j = 25 °C		-	25	mJ
$I_{DS(AL)S}$	non-repetitive avalanche current	unclamped inductive load; V_{DD} ≤ 25 V; R_{GS} = 50 Ω; V_{GS} = 10 V; Figure 4		-	9	A

[1] Mounted to external heatsink, using heatsink compound.



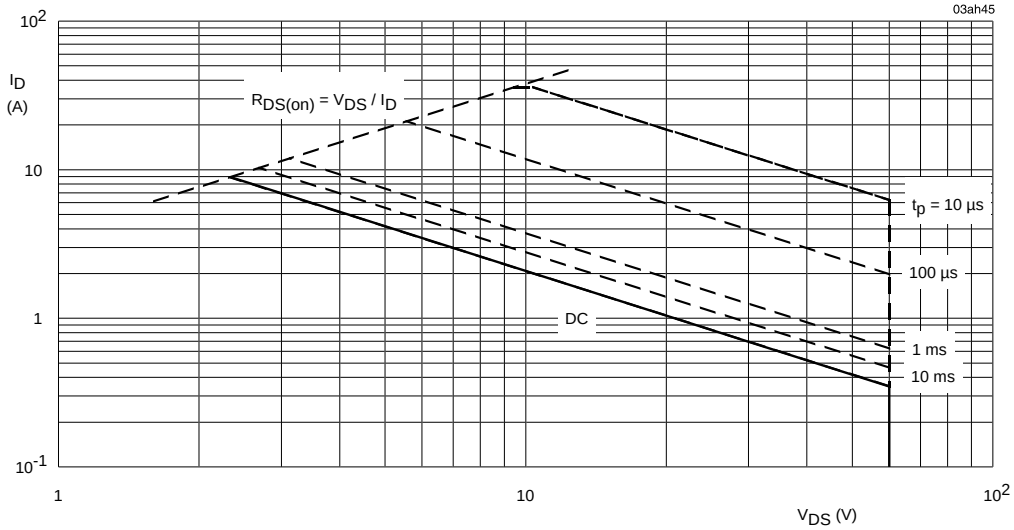
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of external heatsink temperature.



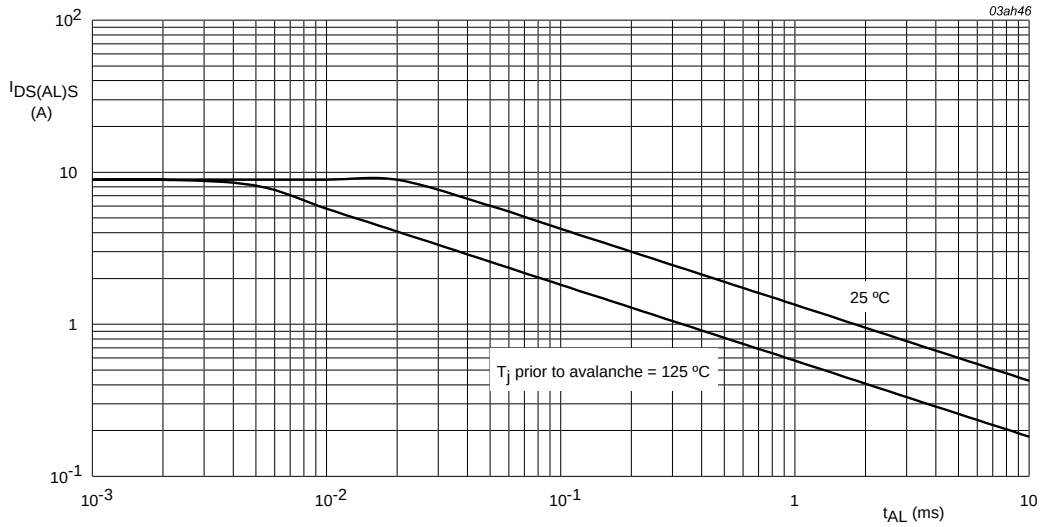
$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of external heatsink temperature.



T_h = 25 °C; I_{DM} is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.



Unclamped inductive load; $V_{DD} \leq 25$ V; $R_{GS} = 50\ \Omega$; $V_{GS} = 10$ V; starting $T_j = 25$ °C and 125 °C.

Fig 4. Non-repetitive avalanche ruggedness current as a function of pulse duration.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	Figure 5	[1]	-	-	6	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in still air		-	55	-	K/W

[1] Mounted to external heatsink, using heatsink compound.

7.1 Transient thermal impedance

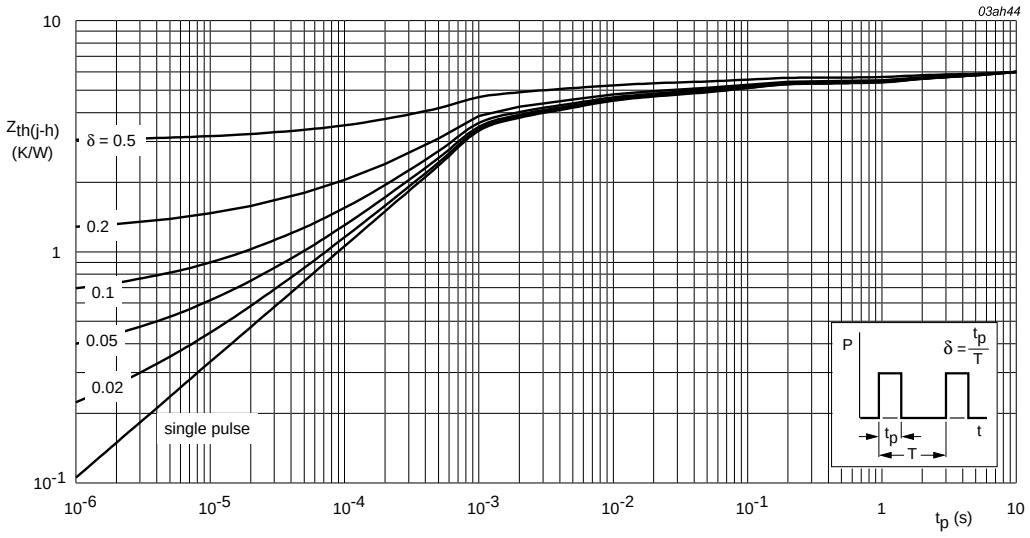


Fig 5. Transient thermal impedance from junction to external heatsink as a function of pulse duration.

8. Isolation characteristics

Table 5: Isolation characteristics

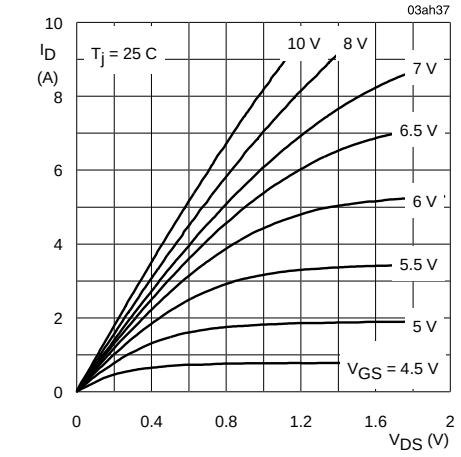
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{isol}	RMS isolation voltage from all three terminals to external heatsink.	f = 50-60 Hz; sinusoidal waveform; RH ≤ 65%; clean and dust-free.	-	-	2500	V
C_{isol}	Capacitance from pin 2 (drain) to external heatsink.		-	10	-	pF

9. Characteristics

Table 6: Characteristics

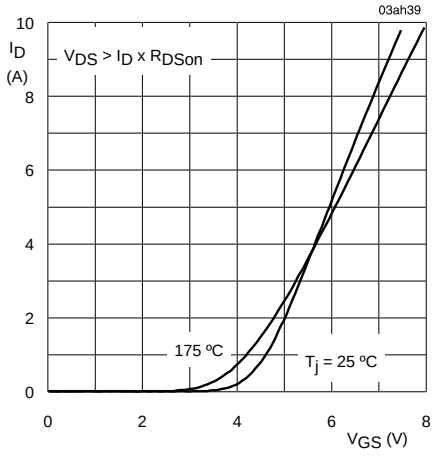
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V				
		T_j = 25 °C	60	-	-	V
		T_j = –55 °C	55	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 10				
		T_j = 25 °C	2	3	4	V
		T_j = 150 °C	1.1	-	-	V
		T_j = –55 °C	-	-	6	V
I_{DSS}	drain-source leakage current	V_{DS} = 55 V; V_{GS} = 0 V				
		T_j = 25 °C	-	0.05	10	µA
		T_j = 150 °C	-	-	100	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 5.5 A; Figure 8 and 9				
		T_j = 25 °C	-	120	150	mΩ
		T_j = 150 °C	-	210	263	mΩ
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	I_D = 10 A; V_{DD} = 44 V; V_{GS} = 10 V; Figure 14	-	5.8	-	nC
Q_{gs}	gate-source charge		-	1.5	-	nC
Q_{gd}	gate-drain (Miller) charge		-	3.2	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; Figure 12	-	190	250	pF
C_{oss}	output capacitance		-	55	80	pF
C_{rss}	reverse transfer capacitance		-	40	50	pF
$t_{d(on)}$	turn-on delay time	V_{DD} = 30 V; R_L = 2.7 Ω; V_{GS} = 10 V; R_G = 5.6 Ω; resistive load	-	3	10	ns
t_r	turn-on rise time		-	26	35	ns
$t_{d(off)}$	turn-off delay time		-	8	15	ns
t_f	turn-off fall time		-	10	20	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 10 A; V_{GS} = 0 V; Figure 13	-	1.1	1.5	V
t_{rr}	reverse recovery time	I_S = 10 A; dI_S/dt = –100 A/µs; V_{GS} = 0 V	-	32	-	ns
Q_r	recovered charge		-	50	-	nC



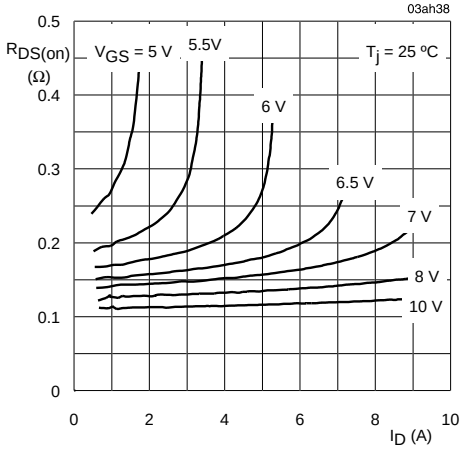
T_j = 25 °C

Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values.



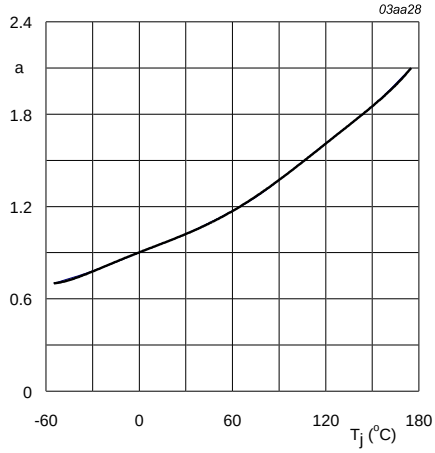
T_j = 25 °C and 175 °C; V_{DS} > I_D x R_{DSon}

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



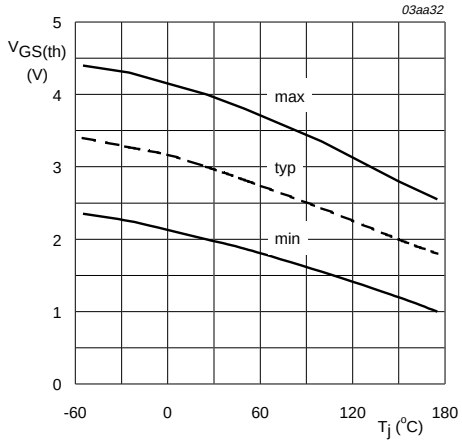
T_j = 25 °C

Fig 8. Drain-source on-state resistance as a function of drain current; typical values.



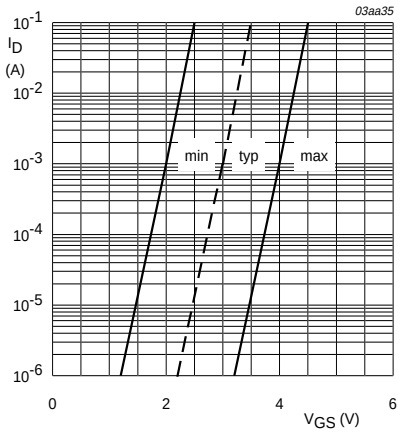
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$

Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature.



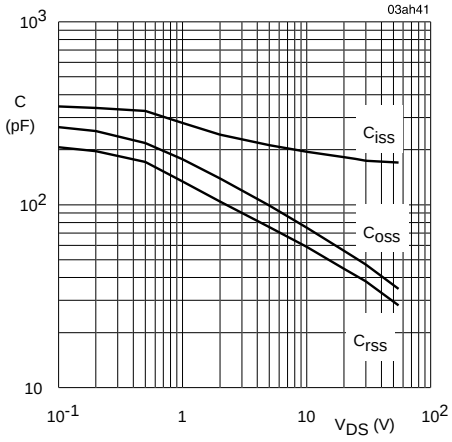
I_D = 1 mA; V_{DS} = V_{GS}

Fig 10. Gate-source threshold voltage as a function of junction temperature.



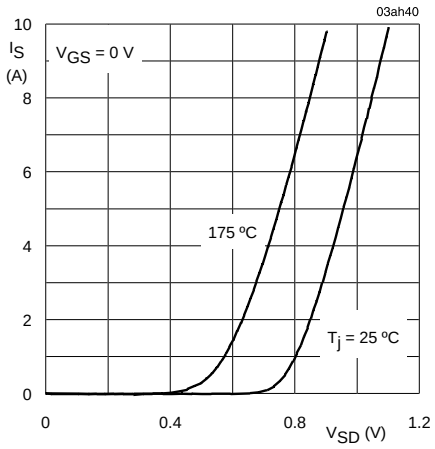
T_j = 25 °C; V_{DS} = 5 V

Fig 11. Sub-threshold drain current as a function of gate-source voltage.



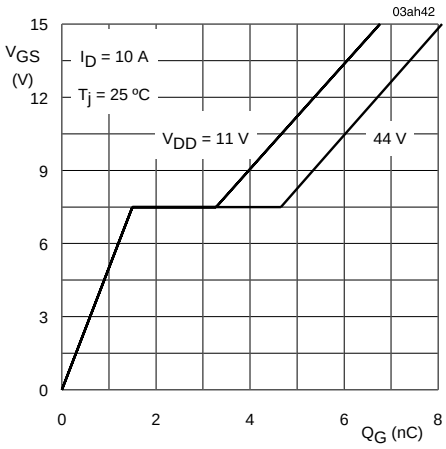
V_{GS} = 0 V; f = 1 MHz

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



T_j = 25 °C and 175 °C; V_{GS} = 0 V

Fig 13. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.

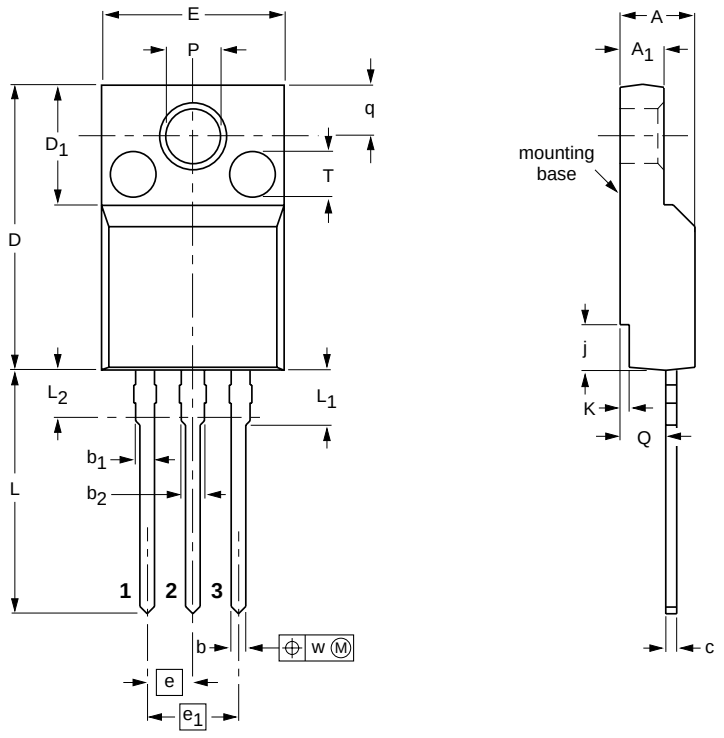


I_D = 10 A; V_{DD} = 11 V and 44V

Fig 14. Gate-source voltage as a function of gate charge; typical values.

10. Package outline

Plastic single-ended package; isolated heatsink mounted;
1 mounting hole; 3 lead TO-220 'full pack' **SOT186A**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	b_2	c	D	D_1	E	e	e_1	j	K	L	L_1	L_2 (1) max.	P	Q	q	T (2)	w
mm	4.6 4.0	2.9 2.5	0.9 0.7	1.1 0.9	1.4 1.2	0.7 0.4	15.8 15.2	6.5 6.3	10.3 9.7	2.54	5.08	2.7 2.3	0.6 0.4	14.4 13.5	3.30 2.79	3	3.2 3.0	2.6 2.3	3.0 2.6	2.5	0.4

Notes

1. Terminal dimensions within this zone are uncontrolled. Terminals in this zone are not tinned.
2. Both recesses are ∅ 2.5 × 0.8 max. depth

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT186A		3-lead TO-220F				~~99-09-13~~ 02-03-12

Fig 15. SOT186A (Isolated TO-220).

11. Revision history

Table 7: Revision history

Rev	Date	CPCN	Description
03	20020318		**Product data (9397 750 09355); supersedes PHX3055E_2 of 8 August 1999** Modifications: • The format of this specification has been redesigned to comply with Philips Semiconductors new presentation and information standard • Changes to Table 2 “Quick reference data” and Table 3 “Limiting values” – Changed value for V_{DS} from 55 V to 60 V – Changed value for V_{DGR} from 55 V to 60 V – Changed “E_{AS}” to “$E_{DS(AL)S}$” – Changed “I_{AS}” to “$I_{DS(AL)S}$” • Removed L_d and L_s entries in Table 6 “Characteristics”: • Removed transconductance graph

12. Data sheet status

Data sheet status[1]	Product status[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

13. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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Date of release: 18 March 2002 **Document order number: 9397 750 09355**